A 60GHz transmitter in 0.18µm Silicon Germanium

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Abstract

Simulated results for a Silicon Germanium transmitter operating at 60GHz are presented. The super-heterodyne transmitter is based on a moving IF architecture with two up-conversion stages. The transmitter includes a baseband to 12 GHz image-reject mixer, a 12 to 60 GHz Gilbert-cell mixer, a passive balun and a power amplifier capable of greater than 13dBm saturated output power. All bias voltages are tuneable using a 3-wire serial interface connected to 4-bit DAC's. Also on-chip is a frequency synthesizer that supplies the LO to both mixers and locks the on-chip 24 GHz VCO to an external source.

1. Introduction

In recent years, publications based on millimetre-wave front-ends for 60 GHz+ wireless systems in affordable technology such as CMOS or SiGe have been prevalent. Integrated systems have been demonstrated by IBM, Caltech and Berkley Wireless research labs among others [1-4].

The move from III-V semiconductors such as GaAs and InP to Si has been fuelled by Si's increasing speed, its low comparative cost and the ease of designing on a single substrate.

This paper explores the design of a 60 GHz transmitter in 0.18µm Silicon Germanium. Higher performance transceivers have been demonstrated in 0.13um Silicon Germanium [5], however the 0.18um process is targeted by this group as the performance is satisfactory for a wireless communication system and the cost is lower.

A method for designing inter-stage matching networks in power amplifiers is shown. This method reduces simulation time, allowing optimisation routines to run more rapidly.

The transmitter was designed using Jazz Semiconductors' SBC18hxl Silicon Germanium process [6]. It has 6 metallisation layers, MIM capacitors and planar inductors. This transmitter is one of the major milestones for this research group on the road to implementing an unlicensed 60 GHz radio for consumer applications [7].

One of the major challenges associated with designing Silicon radios at millimetre-wave frequencies is the design flow. Section 2 looks at extensions made to a standard Silicon design kit in order to design at these frequencies. In Section 3 system components including two up-conversion mixers and the power amplifier are described and simulation results are shown. The entire system is shown in Section 4 along with simulated power consumption figures and system parameters.

2. Extending the component library

To develop an efficient design flow a number of components need to be added to the passive and active device models provided by the foundry. This includes transmission lines and transistor feed networks – these are investigated in the following sub-sections.

2.1. Transmission lines

Transmission lines form an integral part of circuit design at millimetre-wave frequencies. In order to reduce the design time, transmission line models for the process were created using an EM simulator. After these models were created, simple layout rules for the transmission lines were followed and EM simulations were not employed for the remainder of the design process.

By using a transmission line such as a shielded micro-strip that has a large degree of isolation, coupling effects can be minimised and related problems such as feedback and oscillation avoided.

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2.2. Parasitic aware design

Transistor models provided by the foundry do not include any of the parasitics apparent when a device is placed in a real circuit. Capturing these parasitics is important as they affect matching networks and overall circuit performance.

By placing the transistors in a standard feed structure (or access manifold) the parasitics can be extracted at an early stage in the design process [8]. In this design the feed structures were laid out such that they snap together with the transmission lines. For each transistor in the transmitter a R+C+CC parasitic extraction was carried out using Calibre within the Cadence layout environment.

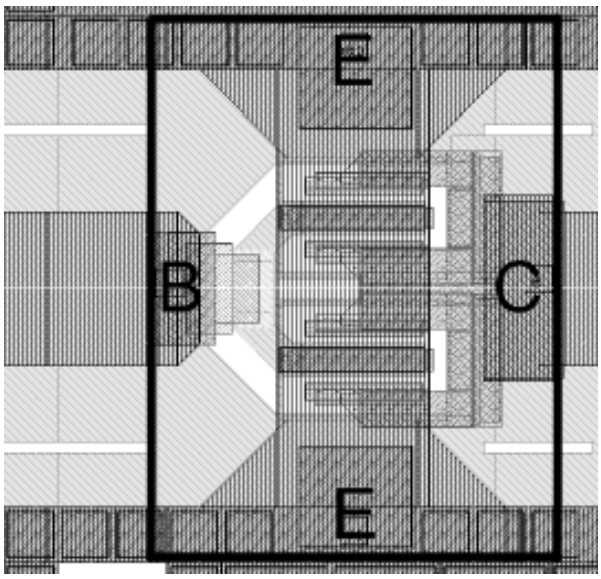

Figure 1. Layout of 2x 10.16µm transistors. The parasitic extraction cell is highlighted. The bases are directly connected to the input transmission line, the collectors are connected to the output transmission line and the emitters are connected to a ground strap.

Figure 1 shows a standard feed structure for a power amplifier transistor. In this cell, two 10.16µm NPN transistors are connected in parallel. This is similar to the way the transistors are laid out in [9]. This cell is designed to join seamlessly with the transmission lines. Layout is made simple by using transmission lines with fixed shield and adjusting the width of the line. The width of the transmission lines including the shield is 50µm.

3. Transmitter components

3.1. Power Amplifier

3.1.1 Overview. The power amplifier shown in Figure 2 consists of 5 stages. A cascode input stage provides 8dB of gain. The final 4 stages are common-emitter amplifiers biased in Class A. Inter-stage matching is carried out using transmission lines and capacitors. The large-signal power gain for the power amplifier is 30dB, it has a 3dB bandwidth of 11.5GHz, centred at 58GHz.

Each bias stage consists of a quarter wavelength transmission line connected to a current source, fed using a 4-bit current-mode DAC. The nominal DAC value is set for maximum gain and can be programmed to output current down to zero allowing the PA to be switched off if needed. The bias networks are cascaded and loadable via a serial control port.

The characteristic impedance for the bias lines was chosen to minimise RF loss and provide maximum isolation. Capacitors are used at the end of the bias lines for RF grounding.

The transistors in the power amplifier have three base and two emitter fingers. This configuration minimises the transit time of electrons between the emitter and collector while maintaining a large emitter area [10]. Using maximum (10.16µm) sized fingers (for this process) in the output stages means that the parasitics in the feed structure can be kept to a minimum (fewer transistors are needed for the same effective emitter length).

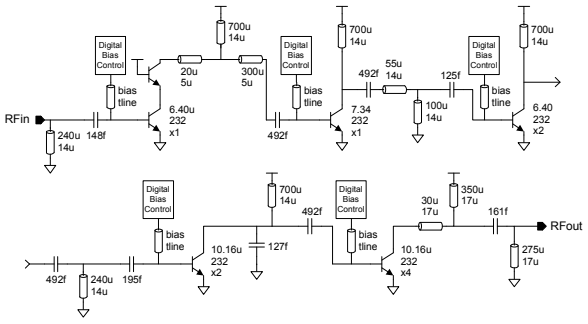

Figure 2. 5-stage power amplifier schematic. The biasing networks have been omitted for clarity.

3.1.2. Matching. Mismatch in a power amplifier contributes to low efficiency, a worsened VSWR, higher die temperature for the same output power and is the cause of many other undesirable effects.

It is not valid to match a power amplifier using small signal S-parameters as the input and output

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characteristics of a HBT change under large-signal conditions. Matching must be done under large signal conditions using a Periodic Steady State (PSS) or Harmonic Balance (HB) simulator.

The problem with PSS and HB simulations is that they are time consuming when compared to an S-parameter analysis. A method was developed to counter this, it allows matching networks to be evaluated and optimised quickly; it is described in the following paragraphs.

For each stage of the design a frequency-domain large signal model of the transistors input impedance with matched output, and output impedance with matched input was created (as the transistors are bilateral in this configuration, mismatch on the output changes the input impedance and vice versa).

The approach is shown in Figure 3. Transistor 1 is to be matched to transistor 2. Circuit 3 is used to model the output impedance of transistor 1. It is generated using an optimisation routine, programmed in visual basic, (within Analog Office) that minimises the mean square error between the real and imaginary components of the large-signal impedance looking into Zout for circuit 1 (Ar) and circuit 2 (Am). The same method is used to model the input of transistor 2 with circuit 4.

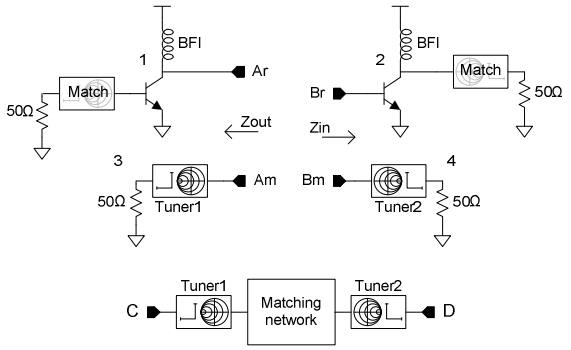

Figure 3. Method to obtain input and output impedance models using Analog Office's frequency dependant tuner model (HBTuner).

By creating these 'impedance models' we can determine the absolute effect of the matching network. To get the best performance out of the power amplifier it is now a process of minimising the loss of the network with a simple simulation instead of undertaking a large-signal analysis of the whole amplifier.

On a stage-by-stage basis we can optimise the inter-stage match and see how it contributes to the overall frequency response of the power amplifier.

The matching networks were optimised using a gradient descent method for low loss (maximum gain). Other factors which were considered were tolerance to manufacturing parameters and low frequency stability.

The output stage was optimised for maximum power transfer using the load-pull wizard in AWR's Analog Office.

All the transmission lines in the power amplifier are shielded micro-strip type with fixed shield and adjustable width, except for the output stage which employs micro-strip lines. Micro-strip lines are used in the output stage as they provide a lower DC resistance for the same characteristic impedance (a 50ohm micro-strip is 17um wide as opposed to 14um for the shielded type).

3.1.3. Layout. Attention was focused on the design of each transistor's feed network. The two critical aims are reducing resistance in series with the base and reducing the base-to-collector capacitance. The resistance in series with the collector while not as critical, must be made as small as possible as it reduces the voltage available to the transistor.

A distributed R+C+CC circuit for each transistor was extracted using Calibre (Mentor Graphics) within the Cadence layout environment.

The power amplifier occupies an area of 870 x 930 μm^2.

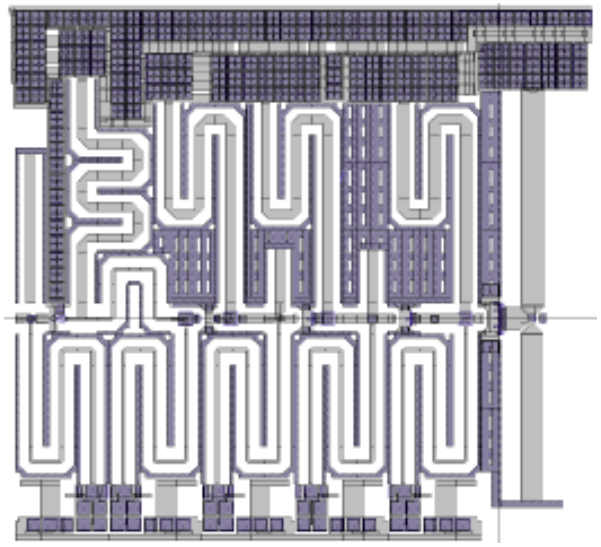

Figure 4. Complete 5-stage power amplifier layout. The input is on the left and output on the right. Bias DACs are along the bottom.

3.1.4. Performance. S-parameter simulation results are shown in Figure 5, the gain peaks slightly lower than

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60GHz due to the output match being designed for maximum power transfer as opposed to maximum gain.

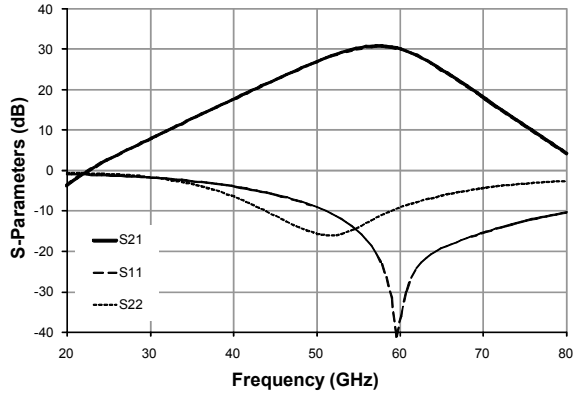

Figure 5. Simulated S-parameters for the power amplifier.

The simulated 1-dB compression point is shown in Figure 6, it is 11.34dBm referred to the output. The saturated output power of the amplifier is greater than 13dBm.

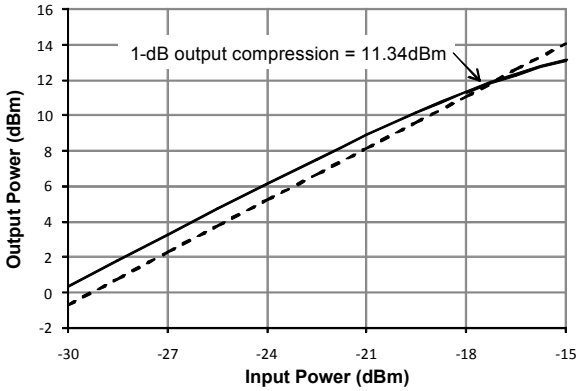

Figure 6. Simulated output compression of the power amplifier.

3.2. Mixer (Base-band – 12 GHz)

The first up-conversion stage employs an image-reject Gilbert cell mixer. To achieve infinite image-rejection the phase of the baseband (BB) I and Q signals must be perfectly quadrature and equal in amplitude. The LO must also have a 90º phase shift. Due to the tolerance and mismatch inherent in the manufacturing process this is not achievable. To maintain 25dB of image-rejection the phase error must be less than ±5º and the amplitude error must be less than 5% [11].

The switching transistors are biased for maximum f_t. This results in a current density of approximately 1mA/micron of emitter length. At this current density the transconductance stage would be twice the size of the switches in order to have the same f_t. However, they are sized 4x larger, this gives a lower noise figure and reduced gain which is optimal for the maximum 2 GHz input frequency. With sufficient LO drive the switching transistors act as ideal switches and do not contribute to the non-linearity of the circuit [12], the transconductance stage is the main non-linear element. To increase the linearity and reduce the gain, emitter degeneration resistors are used.

The transconductance stage is dc coupled to the input transmission lines. This allows the use of high value (1uF) off-chip capacitors for the BB signal which are not achievable on-chip. The input match is obtained using 100 ohm resistors between the differential signal paths.

Inductors are used at the output. This keeps the voltage across transistors at an effective level, allows the output to be tuned to the 12 GHz IF frequency and matched to the following stage. As this design employs a moving IF, the low Q of the on-chip inductors is not a problem and allows a broadband match to be achieved. The inductors were chosen to resonate well away from their self resonant frequency (i.e. approximately 1/3 f_{srf}).

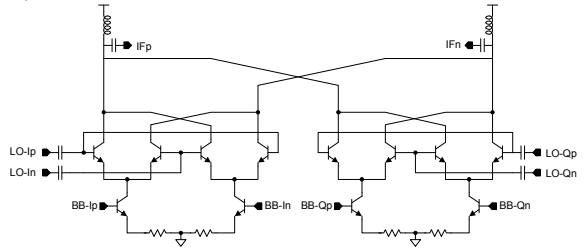

Figure 7. Schematic for BB-to-12G mixer.

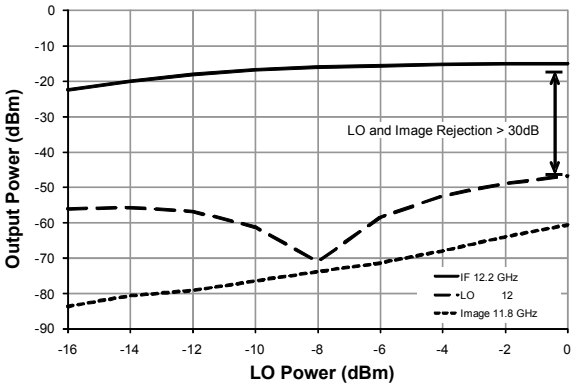

Figure 8. Simulated output for the mixer with swept LO power. Input 200MHz, LO 12GHz.

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Table 1. Mixer simulation results

Conversion Gain (LO >-6dBm)	6dB
LO isolation	> 30dB
Spur isolation	> 30dB
Compression Point (input)	-5dBm

3.3. Mixer 2 (12 – 60 GHz)

The second up-conversion mixer is a Gilbert Cell with tuned input and output. The input is matched to the complex conjugate of the output of the previous mixer. The output is tuned to 50 ohms using a transmission line and capacitor as the passive balun that follows this mixer was designed with 50 ohm single-ended ports.

The image for this mixer is centred around 36 GHz. The tuned output stage attenuates this signal. In the future a notch filter at 36 GHz will be employed to reduce this image further.

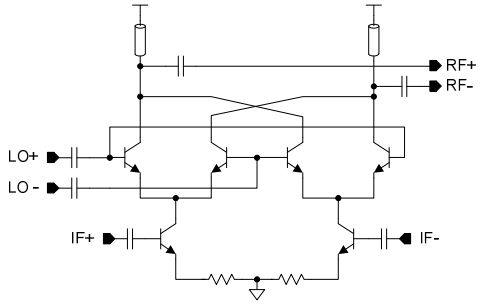

Figure 9. Schematic for 12G-to-60G mixer.

Table 2. Mixer 2 simulation results

Conversion Loss	2dB
LO isolation	> 25dB
Spur isolation	>20dB
Compression Point (input)	-7dBm

4. System

The layout for the entire transmit chain is shown in Figure 10. Each stage is matched to the previous stage using transmission lines and MIM capacitors. The balun between the 60GHz mixer and the power amplifier has been designed with 100Ω differential and 50Ω single-ended ports so the input to the power amplifier is matched to 50Ω.

The transmitter makes use of a differential signal path up to the power amplifier.

The transmitter including the frequency synthesizer occupies 1300 x 2500µm.

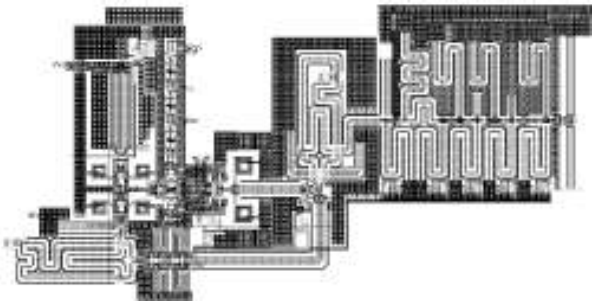

Figure 10. Layout for the entire transmitter. The frequency synthesiser is far left, PA is on the right. The two up-conversion mixers and balun are in the centre.

4.1. System parameters

A plot of the output spectrum with 1GHz baseband input is shown in figure 12. In the future filters will be implemented to meet emission guidelines and reduce the output spectrum at the image (36 GHz) and LO (48 GHz).

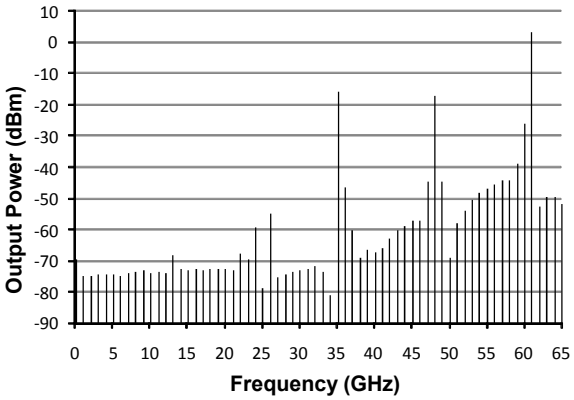

Figure 11. Output spectrum for the transmitter. Input is 1GHz at -25dBm. Both LO's are driven at -3dBm.

Table 3. System parameters

Parameter	Value
Frequency	59-62 GHz
Gain	28-30dB
P1dB output	11dBm
Psat	> 13dBm
Image rejection	>18dB
LO (48GHz) rejection	>20dB

System power consumption values obtained with a transient simulation are shown in table 4.

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Table 4. System power consumption

Component	Voltage (V)	Current (mA)	Power (mW)
Tx (no PA)	1.8	36	100
PA	1.8	208	374
TX	**1.8**	**244**	**439**
Freq Synth	1.8	335	603
Total	**1.8**	**579**	**1042**

5. Conclusion

This paper outlines simulation results for a transmitter designed using 0.18um Silicon Germanium technology for use at 60GHz. The transmitter demonstrates a saturated output power of >13dBm. Without the power amplifier the up-conversion stage consumes 100mW. Including the power amplifier the transmitter consumes 439mW. Future work involves increasing the image-rejection, reducing the LO spurs and DC power consumption.

6. Acknowledgements

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